What is claimed is:

1. A method of manufacturing a semiconductor memory device, comprising the steps of:

forming a trench in an isolation region of a semiconductor substrate and then forming an isolation film within the trench;

forming a screen oxide film on the semiconductor substrate and then forming a triple well through an ion implantation process using a given mask;

removing the screen oxide film, forming a tunnel oxide film and a first polysilicon layer on the entire structure and then patterning the first polysilicon layer to form a floating gate over the semiconductor substrate in the memory cell region;

forming a dielectric film and a second polysilicon layer on the entire structure and then patterning the second polysilicon layer to form a control gate over the semiconductor substrate in the memory cell region;

injecting an ion for controlling the threshold voltage into the exposed semiconductor substrate of the peripheral circuit region; and

forming a gate oxide film and a third polysilicon layer over the semiconductor substrate of the peripheral circuit region, thus forming a gate of a transistor.

2. The method as claimed in claim 1, wherein the triple well includes a triple N well and an N well formed within the triple N well.

3. The method as claimed in claim 2, wherein the triple N well is formed by injecting P31 having the dose of 5E12 ~ 5E13 ion/㎠ with energy of 1000 ~ 2000KeV and the N well is formed by injecting P3 having the dose of 5E12 ~ 5E13 ion/㎠ with energy of 500 ~ 1000KeV.

4. The method as claimed in claim 1, further comprising the step of after the step of forming the triple well, injecting an inert ion into a given depth of the semiconductor substrate and then implementing a rapid thermal process to form an ion implantation layer.

5. The method as claimed in claim 4, wherein the inert ion is nitrogen (N_2) and is injected with energy of 30 ~ 100KeV ad the dose of 1E13 ~ 5E14 ion/㎠.

6. The method as claimed in claim 4, wherein the rapid thermal process is implemented under nitrogen (N_2) atmosphere at a temperature of 900 ~ 1100℃ for 5 ~ 30 seconds.

7. The method as claimed in claim 1, further comprising the step of before the tunnel oxide film is formed, cleaning the surface of the semiconductor substrate using a dilute HF and SC-1 solution.

8. The method as claimed in claim 1, wherein the tunnel oxide film is formed by means of a wet oxidization process using hydrogen (H_2) and

oxygen (O_2) at a temperature of 750 ~ 800℃.

9. The method as claimed in claim 1, wherein the first polysilicon layer is formed by means of a low-pressure chemical vapor deposition method using silicon source gas such as SiH_4 or Si_2H_6 and $POCl_3$ or PH_3 gas at a temperature of 510 ~ 550℃ and a pressure of 0.1 ~ 3.0Torr..

10. The method as claimed in claim 1, wherein the second polysilicon layer is formed by means of a low-pressure chemical vapor deposition method using silicon source gas such as SiH_4 or Si_2H_6 and PH_3 gas at a temperature of 530 ~ 550℃ and a pressure of below 1Torr..

11. The method as claimed in claim 1, wherein the ion for controlling the threshold voltage is BF_2 and is injected with energy of 10 ~ 50KeV at the dose of 1E11 ~ 1E14 ion/㎠.